Multiclock Design and Synthesis with Esterel
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Abstract:

Esterel is a high-level synchronous programming language especially well-suited to embedded hardware development. Its most recent version, Esterel v7, is targeted for hardware design, verification, and synthesis. It is supported by the Esterel Studio toolset which provides its user with textual and graphical design capture, graphical interactive simulation, and formal verification. Texas Instruments is currently using Esterel in projects, ranging from IP design and verification to architectural prototyping.

Esterel was originally designed for single-clock applications. However, modern designs often rely on multiple asynchronous clock domains linked by devices called synchronizers. Several theoretical multiclock extensions have been proposed for Esterel, but all of them rely on unrealistic theoretical synchronizers, ignoring practical metastability issues and synchronization delays.

This paper presents a practical and proven methodology to deal with multiclock designs using Esterel. The key idea is to view domain clocks as signals acting as subclocks of a fictitious primary clock representing the union of them. Clocks zones are then designed as separate single-clock Esterel programs. Clock zone activity is modeled using the Esterel primitive suspension statement. Synchronizers are modeled by Esterel devices acting on the fictitious main clock. The design can thereby be simulated, debugged, and verified using Esterel Studio. When performing synthesis, the Esterel designs for each clock domain are separately synthesized to VHDL in single-clock mode. The obtained VHDL modules are then linked together by manually written VHDL wrapping code containing the clock definitions and the actual synchronizers.

We present two examples of the application of this methodology at Texas Instruments: an example of a handshake protocol to safely exchange a data bus between two clock domains; and a video device with three clock zones. Both designs have been entirely programmed and simulated with Esterel Studio. For the video device, the three clock domains were synthesized using the Esterel optimizing compiler. After the manual connection of the generated modules, the design was validated as the parallel manual design, and no flaw was found. In addition, the resulting Esterel-generated multiclock circuit was 5% smaller than the manually designed one for the same speed synthesis constraints

The success of the TI projects suggests a generic methodology for automating multiclock design using Esterel.

Plan of the paper

1. Introduction (modified abstract content)
2. Brief overview of Esterel and Esterel Studio
3. Multiclock design
   - The need for clock zones
   - Metastability issues
   - How to build synchronizers
4. Modeling clock zones and synchronizers on Esterel
   - Using suspension for clock zones
   - Modeling synchronizers
5. Experimental results
   - The MSB/LSB protocol
   - The video unit
6. Conclusion